IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): G.A. Bouchard et al.
Case: 3-7-4-4-7-2
Serial No.: 10/029,679
Filing Date: December 21, 2001
Group: 2152
Examiner: Lan Dai T. Truong

Title: Methods and Apparatus for Using Multiple Reassembly Memories for Performing Multiple Functions

---

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter referred to as "Appellants") hereby appeal the final rejection of claims 1-9 and 11-20 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded March 15, 2002 in the U.S. Patent and Trademark Office at Reel 12703, Frame 111. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

Claims 1-9 and 11-20 stand finally rejected under 35 U.S.C. §103(a). Claim 10 is canceled. Claims 1-9 and 11-20 are appealed.

STATUS OF AMENDMENTS

An amendment was filed subsequent to the final rejection on September 14, 2006. The amendment corrected the dependency of claim 12 to overcome an objection. Since there is no negative indication in the Advisory Action with regard to entry of the filed amendment, Applicants assume that the amendment was entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a processing system comprising first processing circuitry for performing a first function; first reassembly circuitry, associated with the first processing circuitry, for reassembling segments of received packets into reassembled packets, the segments to be reassembled being related to the first function; first memory circuitry, associated with the first processing circuitry, for storing the packets reassembled by the first reassembly circuitry, wherein the reassembled packets stored by the first memory circuitry are used by the first processing circuitry in accordance with the first function; at least second processing circuitry for performing a second function; at least second reassembly circuitry, associated with the second processing circuitry, for reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to the second function; and at least second memory circuitry, associated with the second processing circuitry, for storing the packets reassembled by the second reassembly circuitry, such that at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same, wherein the reassembled packets stored in the second memory circuitry are used by the second processing circuitry in accordance with the second function.. The present specification provides an illustrative embodiment of the elements of claim 1 at page 4, line 21 through page 5, line 14.

More particularly, FIG. 1 shows a packet processing system 100 employing multiple reassembly memories according to an embodiment of the present invention. The system 100 includes a cell parser 102 and N packet processors 104-1 through 104-N, where N may be an integer equivalent to the number of processors that the processing system 100 is designed to support. Each

packet processor104 includes a packet or PDU reassembler 106 (106-1 through 106-N) and a PDU memory 108 (108-1 through 108-N). Each processor also has at least one packet-related function 110 (110-1 through 110-N) associated therewith. It is to be understood that each processor may perform more than one function and that any two processors may perform distinct portions of the same function. Also, each of the N processors may be implemented on N, more than N, or less than N, integrated circuits or processing devices (including one integrated circuit or processing device). Further, the packet processing system 100 may be implemented in a router or other type of packet switch. In such case, the functions to be performed by the respective processors in accordance with their respective reassembly memories may be, by way of example and without limitation, packet classification, packet scheduling, etc.

Advantageously, as shown, the packet processing system 100 is designed such that the memory required to perform the N functions is partitioned into N memories (108-1 through 108-N) which respectively provide enough bandwidth to reassemble the same data, or at least a selection of required data, to perform the corresponding function. Thus, the data may be reassembled and stored in parallel in each of the N memories. The parallel operations may be simultaneous or substantially simultaneous (e.g., delayed by some amount of time). (Specification, page 4, line 21 through page 5, line 14).

Independent claim 15 is a method claim having similar elements as the above-described claim 1. Support for claim 15 is also shown at page 4, line 21 through page 5, line 14.

Independent claim 18 is an apparatus claim having similar elements as the above-described claim 1. The apparatus comprises a processor and memory arrangement. FIG. 1 shows an illustrative hardware implementation of a packet processing system 100 employing multiple reassembly memories according to an embodiment of the present invention. The system 100 includes a cell parser 102 and N packet processors 104-1 through 104-N, where N may be an integer equivalent to the number of processors that the processing system 100 is designed to support. Each packet processor 104 includes a packet or PDU reassembler 106 (106-1 through 106-N) and a PDU memory 108 (108-1 through 108-N). (Specification, page 4, lines 21-26).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(I) Whether claims 1-3, 6 and 11-20 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,623,494 (hereinafter "Rostoker") in view of U.S. Patent No. 6,934,760 (hereinafter "Westbrook").

(II) Whether claim 4 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,149,243 (hereinafter "Wallis").

(III) Whether claim 5 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,593,357 (hereinafter "Ostrand").

(IV) Whether claim 7 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,058,114 (hereinafter "Sethuram").

(V) Whether claims 8 and 9 are unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,483,839 (hereinafter "Gemar").

ARGUMENT

Appellants incorporate by reference herein the disclosure of their previous response filed in the present application, namely, the response dated September 14, 2006.

(I) Whether claims 1-3, 6 and 11-20 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,623,494 (hereinafter "Rostoker") in view of U.S. Patent No. 6,934,760 (hereinafter "Westbrook").

Regarding the §103(a) rejections, Appellants assert that the various references, alone or in combination, fail to teach or suggest all of the limitations of claim 1-9 and 11-20, as will be explained below. Furthermore, with regard to the combinations of the various references, Appellants assert that such combinations are improper, as will be explained below.

The Examiner cites Rostoker in combination with Westbrook in rejecting independent claims 1, 15 and 18. More particularly, the Examiner cites portions of Rostoker as disclosing certain limitations of the independent claims, and cites portions of Westbrook as disclosing certain other

limitations of the independent claims. Below, Appellants explain how such portions of Rostoker and Westbrook fail to teach or suggest what the Examiner contends that they teach or suggest. While Appellants may refer from time to time to each reference alone in describing its deficiencies, it is to be understood that such arguments are intended to point out the overall deficiency of the cited combination.

In characterizing the Rostoker reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on the abstract, lines 1-28; column 3, lines 34-47; column 4, lines 20-26; column 6, lines 48-67; and figure 2. However, the relied-upon portions of Rostoker fail to teach or suggest the limitations as alleged. The relied-upon portions of Rostoker state that each ATM termination unit 50 includes a processor for segmenting and reassembling the ATM cells and that each ATM terminal unit interfaces with a host unit 102. The Examiner seems to consider two of the host units to be the claimed "first processing circuitry" and "second processing circuitry," as well as the "first memory circuitry" and "second memory circuitry." Further, the Examiner seems to consider two of the ATM terminal units to be the claimed "first reassembly circuitry" and "second reassembly circuitry."

However, even assuming this is the case for the sake of argument, no where does Rostoker disclose that the second reassembly circuitry, associated with the second processing circuitry, reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to a second function (whereas the segments reassembled by the first reassembly circuitry are related to a first function), as recited in the independent claims. That is, no where does Rostoker state that one ATM terminal unit reassembles at least a portion of the same segments of packets reassembled by another ATM terminal unit.

The Examiner states on page 3 of the final Office Action that "applicant does not clearly disclose if the first function and second function are distinct; so they could execute the same job/or task." However, this is not relevant to the claimed limitation. The claimed limitations recites that the second reassembly circuitry reassembles at least a portion of the same segments of packets

reassembled by the first reassembly circuitry. The claim expressly recites a limitation with respect to the sameness of the packets, not the sameness of the first and second functions.

The Westbrook reference fails to supplement the above-noted deficiencies of Rostoker as applied to claim 1.

In characterizing the Westbrook reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on column 7, lines 22-27 and lines 55-60, of Westbrook. However, the relied-upon portions of Westbrook fail to teach or suggest the limitations as alleged. The relied-upon portions of Westbrook appear to relate to distributed resequencing and/or reassembling components resequencing and/or reassembling packets. For example, Westbrook at column 7, lines 22-27, provides as follows:

> Moreover, these distributed resequencing and/or reassembly components 203A-N may resequence and/or reassemble a single stream of packets, or typically in a large system simultaneously resequence and/or reassemble one or more streams of packets.

In addition, Westbrook, at column 7, lines 55-60, provides as follows:

> Distributed resequencing and/or reassembly components 203A-N coordinate the resequencing and/or reassembly process(es) typically by sharing information as to what packets are currently held by each of the distributed resequencing and/or reassembly components 203A-N, and coordinating the sending of packets over a packet merge bus 209 (or other communications mechanism) to produce one or more streams of resequenced and/or reassembled packets.

There is no description in the relied-upon portion of Westbrook relating to, for example, the claimed features of: "at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same."

That is, while Westbrook describes multiple components for resequencing and/or reassembling packets, it is clear that Westbrook is not stating that any two components reassemble the same packets. In fact, it is clear from Figure 2A and 2b of Westbrook (and the related textual description) that Westbrook is solving the "out-of-sequence" problem (see column 1 of Westbrook) that occurs when individual packets from one or more data streams are separated so they can be individually routed on different network paths in order to get to a single destination more efficiently.

Thus, distributors 200 shown in Figures 2A and 2B are understood to distribute different packets to each component 203. In fact, if the same packets could be distributed to each component (as the Examiner seems to suggest), there would be no need for the components to communicate between one another as to which packets each component received (see column 8, lines 9-11 of Westbrook).

In the Advisory Action, the Examiner again states that Westbrook "discloses method for sending packets of data into multiple 'reassembly units' those [sic] are equivalent to 'reassembly circuitries', then the 'reassembled packets' those [sic] are equivalent to 'portion of segments of packets' sent to another reassembly unit, see (column 4, lines 50-60, lines 1-25; column 5, lines 1-13; column 7, lines 22-27, 55-60; column 3, lines 40-55)." Furthermore, the Examiner again states in the Advisory Action that "Applicant does not state that the first memory circuitry and the second memory circuitry are distinct as claimed," and points to column 5, lines 1-12 of Westbrook as disclosing at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same. Again, as noted above, while Westbrook describes multiple components for resequencing and/or reassembling packets, Westbrook does not state that any two components reassemble the same packets.

The Rostoker reference fails to supplement the above-noted deficiencies of Westbrook as applied to claim 1. Accordingly, it is believed that the combined teachings of Rostoker and Westbrook fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining Rostoker and Westbrook in the manner proposed. The Examiner provides the following statement of motivation at page 4, second paragraph of the Office Action:

> Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of a plurality of reassembly components may reassemble a single stream of packets with Rostoker's system in order to provide an improved reassembling system: (Rostoker: column 3, lines 14-26)

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su

Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine Rostoker and Westbrook to produce the particular limitations in question. The above-quoted statement of motivation provided by the Examiner appears to be a conclusory statement of the type ruled insufficient in the In re Sang-Su Lee case. Accordingly, the proposed combination appears to be based primarily on hindsight, with the Examiner attempting to reconstruct the claimed arrangement from disparate references.

For at least these reasons, Appellants assert that independent claim 1 is patentable over the Rostoker/Westbrook combination. Independent claims 15 and 18 include limitations similar to those of claim 1, and are therefore believed patentable for reasons similar to those described above with reference to claim 1. Furthermore, Appellants assert that the claims which depend from claim 1 are patentable over the Rostoker/Westbrook combination not only for the reasons given above with respect to claim 1, but also because such dependent claims recite patentable subject matter in their own right, as will be set out below.

Regarding claims 2, 16 and 19, the Rostoker/Westbrook combination does not teach or suggest "the first processing circuitry, the first reassembly circuitry, the first memory circuitry, the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on an integrated circuit." The Examiner again states that "applicant does not clearly disclose if first function and second function are distinct; so they could execute the same job/or task," at page 5, first paragraph of the final Office Action. As noted above, this is not relevant to the claimed limitation. Independent claims 1, 15 and 18, from which claims 2, 16 and 19 depend from respectively, recite that the second reassembly circuitry reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry, which is a limitation with respect to the sameness of the packets, not the sameness of the first and second functions.

Regarding claims 3, 17 and 20, Rostoker does not teach or suggest "the first processing circuitry, the first reassembly circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on a second integrated circuit." As noted above, assuming for the sake of argument that the host units of Rostoker are the claimed first and second processing circuitry as well as the first and second memory circuitry, and the ATM terminal units are the claimed first and second reassembly circuitry, no where does Rostoker state that one ATM terminal unit reassembles at least a portion of the same segments of packets reassembled by another ATM terminal unit.

Regarding claim 11, neither Rostoker nor Westbrook teach or suggest of "parsing circuitry... for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets."

(II) Whether claim 4 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,149,243 (hereinafter "Wallis").

Appellants assert that claim 4, which depends from claim 1, is patentable over the Rostoker/Westbrook/Wallis combination not only for the reasons given above with respect to claim 1, but also because claim 4 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Wallis with Rostoker and Westbrook is insufficient under the In re Sang-Su Lee decision (cited above).

(III) Whether claim 5 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,593,357 (hereinafter "Ostrand").

Appellants assert that claim 5, which depends from claim 1, is patentable over the Rostoker/Westbrook/Ostrand combination not only for the reasons given above with respect to claim 1, but also because claim 5 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Ostrand with Rostoker and Westbrook is insufficient under the In re Sang-Su Lee decision (cited above).

(IV) Whether claim 7 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,058,114 (hereinafter "Sethuram").

Appellants assert that claim 7, which depends from claim 1, is patentable over the Rostoker/Westbrook/Sethuram combination not only for the reasons given above with respect to claim 1, but also because claim 7 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Sethuram with Rostoker and Westbrook is insufficient under the In re Sang-Su Lee decision (cited above).

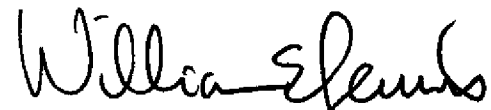
(V) Whether claims 8 and 9 are unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,483,839 (hereinafter "Gemar").

Appellants assert that claims 8 and 9, which depend from claim 1, are patentable over the Mishra/Tenev combination not only for the reasons given above with respect to claim 1, but also because such dependent claims recite patentable subject matter in their own right.

It is also asserted that the motivation set forth by the Examiner to combine Gemar with Rostoker and Westbrook is insufficient under the In re Sang-Su Lee decision (cited above).

In view of the above, Applicants believe that claims 1-9 and 11-20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,



Date: January 16, 2007

William E. Lewis
Attorney for Applicant(s)
Reg. No. 39,274
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-2946

APPENDIX

1. A processing system comprising:

first processing circuitry for performing a first function;

first reassembly circuitry, associated with the first processing circuitry, for reassembling segments of received packets into reassembled packets, the segments to be reassembled being related to the first function;

first memory circuitry, associated with the first processing circuitry, for storing the packets reassembled by the first reassembly circuitry, wherein the reassembled packets stored by the first memory circuitry are used by the first processing circuitry in accordance with the first function;

at least second processing circuitry for performing a second function;

at least second reassembly circuitry, associated with the second processing circuitry, for reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to the second function; and

at least second memory circuitry, associated with the second processing circuitry, for storing the packets reassembled by the second reassembly circuitry, such that at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same, wherein the reassembled packets stored in the second memory circuitry are used by the second processing circuitry in accordance with the second function.

2. The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry, the first memory circuitry, the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on an integrated circuit.

3. The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second

processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on a second integrated circuit.

4. The system of claim 1 wherein the first function and the second function are performed by an integrated circuit.

5. The system of claim 1 wherein the first function and the second function are performed by different integrated circuits.

6. The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry and the first memory circuitry comprise a network processor.

7. The system of claim 6 wherein the first function comprises a packet classifying operation.

8. The system of claim 1 wherein the second processing circuitry, the second reassembly circuitry and the second memory circuitry comprise a traffic manager.

9. The system of claim 8 wherein the second function comprises a packet scheduling operation.

11. The system of claim 1 further comprising parsing circuitry, coupled to the first reassembly circuitry and the second reassembly circuitry, for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets.

12. The system of claim 1 wherein the packet segments are cells.

13. The system of claim 1 wherein the first processing circuitry and the second processing circuitry operate in a packet switching device.

14. The system of claim 13 wherein the first processing circuitry and the second processing circuitry operate between a packet network interface and a switch fabric of the packet switching device.

15. A method for use in a processing system wherein the processing system is responsive to packets, the method comprising the steps of:

reassembling segments of received packets into reassembled packets in a first reassembler, wherein the segments being reassembled are related to a first function; and

storing the reassembled packets in a first memory, the reassembled packets stored by the first memory are used by a first processor in accordance with the first function;

wherein at least a portion of the segments of received packets reassembled by the first reassembler may be reassembled in at least a second reassembler for storage in at least a second memory usable by at least a second processor in accordance with a second function, such that at least a portion of the reassembled packets stored in the first memory and the second memory are the same.

16. The method of claim 15 wherein the first reassembler, the first processor, the first memory, the second reassembler, the second processor and the second memory are implemented on an integrated circuit.

17. The method of claim 15 wherein the first reassembler, the first processor and the first memory are implemented on a first integrated circuit, and the second reassembler, the second processor and the second memory are implemented on a second integrated circuit.

18. Apparatus for use in a processing system wherein the processing system is responsive to packets, the apparatus comprising:

a first memory; and

a first processor operative to: (I) reassemble segments of received packets into reassembled packets, wherein the segments being reassembled are related to a first function; and (ii) cause the storage of the reassembled packets in the first memory, the reassembled packets stored by the first memory are used in accordance with the first function;

wherein at least a portion of the segments of received packets reassembled by the first processor may be reassembled by at least a second processor for storage in at least a second memory usable in accordance with a second function, such that at least a portion of the reassembled packets stored in the first memory and the second memory are the same.

19. The apparatus of claim 18 wherein the first processor and the first memory, the second processor and the second memory are implemented on an integrated circuit.

20. The apparatus of claim 18 wherein the first processor and the first memory are implemented on a first integrated circuit, and the second processor and the second memory are implemented on a second integrated circuit.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.